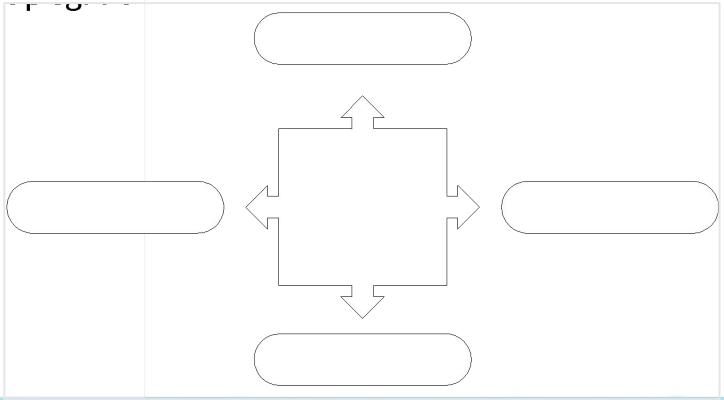
DESIGN-FOR-VERIFICATION

– RETURN ON INVESTMENT

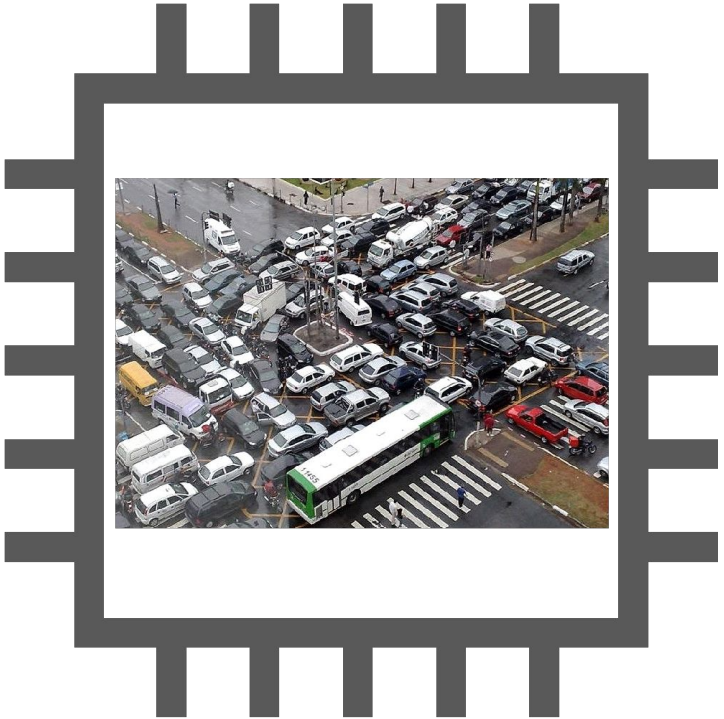
ADDRESSING CHALLENGES in SoC DV

Rising complexity and challenges in SoC DV and emulation - “As expensive to verify the chip as fabricate it”

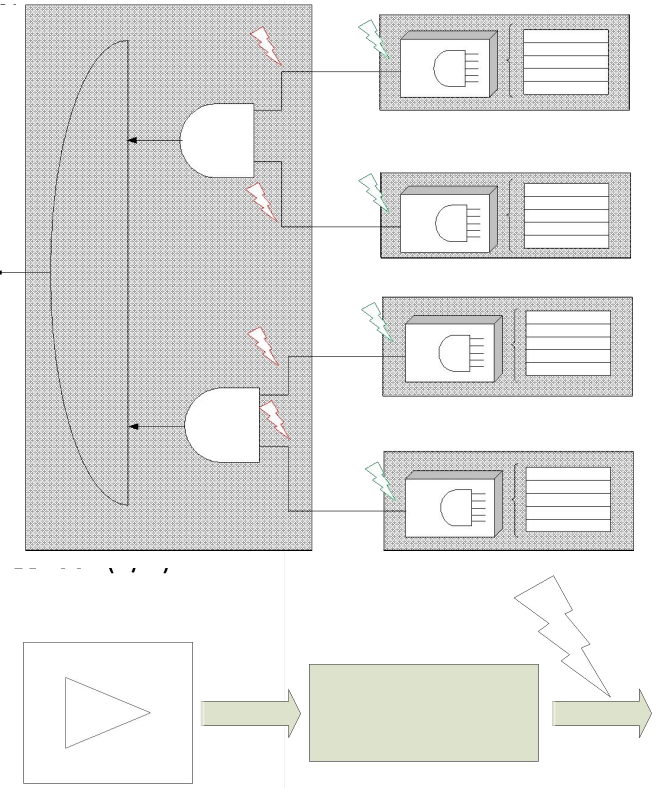
- ❑ Ever-increasing complexity of SoCs
- ❑ Dependence on later-stage IPs maturity
- ❑ Ever-increasing drain on IP teams resources
- ❑ Not all tests can be reused across IP DV/SoC DV/Emulation/bring-up



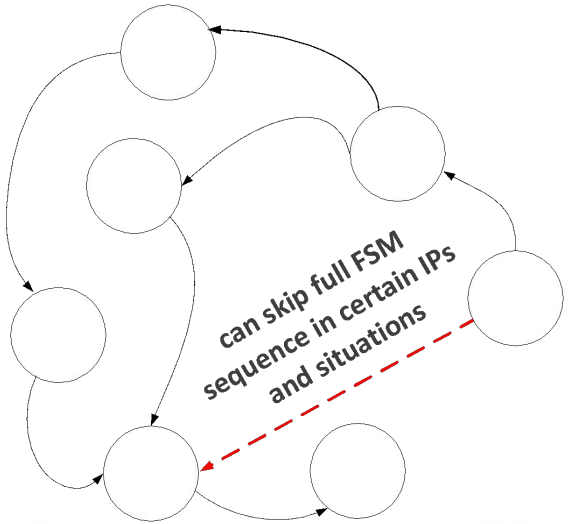
“Resolving SoC DV deadlocks”



DfV - WHAT IS DESIGN-FOR-VERIFICATION?



- Adding HW to assist verification
- Trigger situations which are hard to achieve
- Isolate the process of interest




```
module cntr(clk,reset,load,in,count);
input clk, reset, load;
input [7:0] in;
output [7:0] count;
reg [7:0] count;
always @ (posedge clk)
if (reset) count=0;
else
if (load) count=in;
else if (count==255) count=0;
else count=count+1;
endmodule
```

DfV – APPLICATION AREAS

Some of application areas for DfV
DfV for emulation
DfV for analog components and PHYs
DfV for enabling multi-die DV
DfV for control sequences bypass or override
DfV for backpressure and flow control
DfV for DFT and DFD
DfV for Power management

What do we achieve?

- Compartmentalization

- Bypass in-depth IP sequences

- Handling elements not present in simulated configurations

- Improve DV fidelity of configurations involving analog elements

- Arrive at hard-to-achieve states

- observability, controllability and state isolation

DESIGN FOR VERIFICATION VS. OTHER APPROACHES

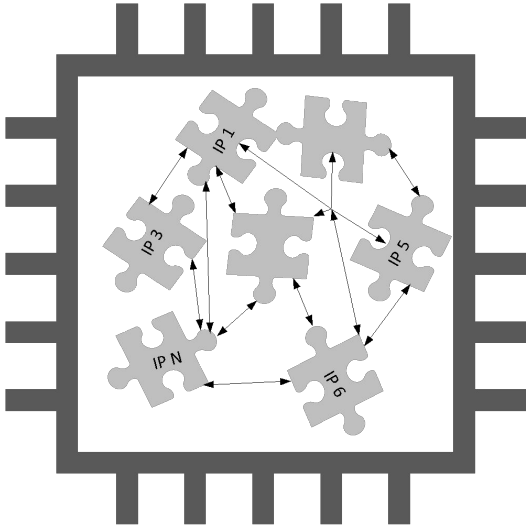
	DfV	DFT	DFD
Addresses (3rd party) IPs and PHYs pre-silicon integration	YES	NO	NO
Addresses pre-silicon SoC Verification	YES	NO	NO
Addresses Emulation	YES	NO	NO
Benefits chip test, bring-up and validation	Indirectly	YES	YES
Amount of HW involved	**Low to medium**	Medium to high	Medium to high
Needs STA convergence	Mostly NO	YES	YES
Resources required for the pre-silicon DV	LOW	YES	YES

DfV – how can it be defined?

- ✔ Many available H/W solutions in SoCs belong to DfV area w/o being labelled as such, e.g. state overrides
- ✔ Investment in DfV indirectly benefits other areas – DFT, DFD, and many others, however, as a by-product
- ✔ Need a change of mindset to prioritize DfV

DfV: BENEFITS and ROI

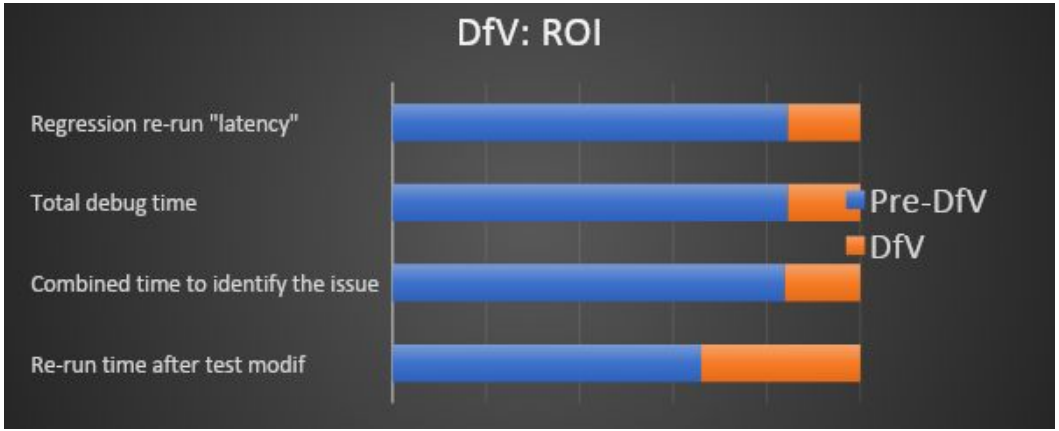
- ✔ Avoids delaying the bulk of DV work until late stages of the project
- ✔ Shift-Left for complex multi-die SoC projects; mitigates tape-out delays
- ✔ Significant reduction in test run times
- ✔ Improved verification fidelity
- ✔ Avoids late-stage issues discoveries, especially in complex configurations
- ✔ Reduces the likelihood of bug escapes by shifting left the SoC DV
- ✔ Enables IP DV, SOC DV and bring-up testcase reuse



DfV – Return on Investment (ROI)

Re-run time after test changes (1) re-build (2) re-run → Time to find the issue after testcase run → Re-run cycles to identify the issue → Combined time (human + machine) to identify the issue → Overall machine & debug hours

- Re-run time is reduced
- Issue identification time reduced
- Re-run cycles required to identify the issue reduced
- Total debug time reduced



CONCLUSIONS

- DfV – a valuable tool (or philosophy) for modern chip design and DV
- DfV benefits multiple stakeholders if planned well
- Required awareness among Architects, Designers and DV Community
- Unification of DfV approaches and best practices are important
- DfV pays off
- Need a change of mindset to prioritize DfV

THANK YOU!

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